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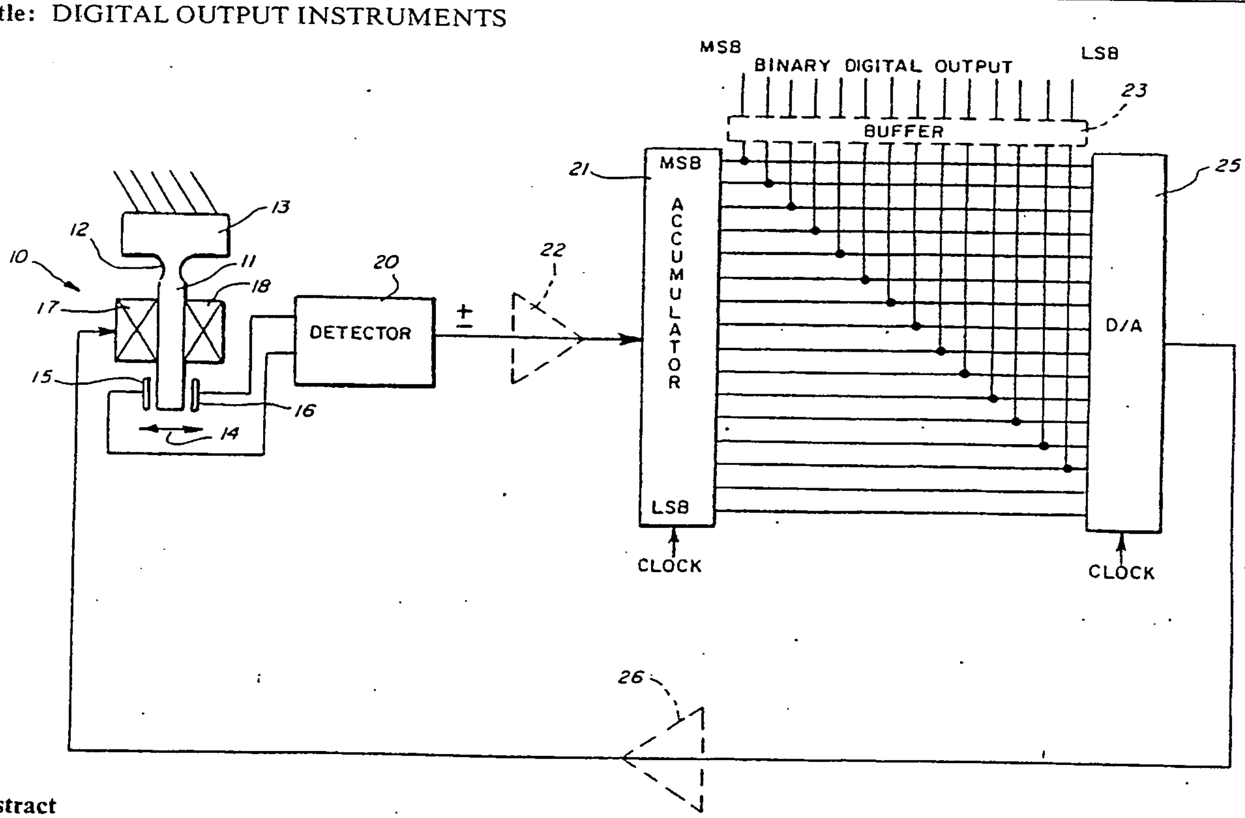
(54) Title: DIGITAL OUTPUT INSTRUMENTS



(57) Abstract

A servoed accelerometer (10) is connected with an accumulator (21) to provide a binary digital output. The accumulator output is connected with a digital-to-analog converter (25) which provided an analog rebalance signal to the accelerometer.

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DIGITAL OUTPUT INSTRUMENT

Technical Field

This invention relates to a measuring instrument, as a servoed accelerometer, with a digital output.

Background of the Invention

Typical accelerometers have an analog output of current, voltage or frequency. In order to interface such an instrument with a digital computer, the analog signal must be converted to digital form. For the current and voltage instruments, this is generally accomplished with an analog-to-frequency converter. In the case of a frequency output accelerometer or a voltage-to-frequency conversion, a computer or other frequency measurement is required to generate a digital output. In an open loop configuration, such an instrument is nonlinear. In a closed loop instrument, the output has a high noise level and different scale factors for positive and negative inputs.

Summary of the Invention

In accordance with the present invention, a servoed instrument has a displaceable element with means for applying force to the element to return the element to its null position. A detector responsive to displacement of the element from the null position has an analog output signal with a polarity which indicates the direction of displacement and an amplitude which represents the

magnitude of the displacement. An analog-to-digital converter is responsive to the detector output signal and has a digital output representing the sensed stimulus to which the element responds. A digital-to-analog converter has an input connected with the output of the analog-to-digital converter and an analog output connected with the displacement element forcer to return the element to the null position. The digital output of the analog-to-digital converter provides an instrument output which is computer compatible.

More particularly, the analog-to-digital converter is an accumulator, the output of which is one-half full count for a null condition in the absence of a stimulus acting on the displacement element and which increments for one polarity of detector output signal and decrements for the opposite polarity of detector output signal.

Another feature of the invention is that the digital-to-analog converter has a bipolar analog output which is zero for one-half full scale digital input.

Further features and advantages of the invention will readily be apparent from the following specification and from the drawing which is a schematic representation of a servoed accelerometer and a digital output circuit illustrating the invention.

The invention is illustrated and will be described as incorporated in a force rebalance or servoed accelerometer. Various aspects of the invention may be used with other digital instruments having an element displaceable from a null position in response to a sensed stimulus. The claims should not be considered limited to an accelerometer or to other details of the disclosure unless expressly so stated.

Accelerometer 10 has a proof mass element 11 connected by a hinge section 12 with a base 13. Proof mass 11 is displaceable in opposite directions from its null or rest position in response to an acceleration having a component in the direction of double ended arrow

14. Movement of the element 11 is sensed as by the differential capacitors including plates 15, 16 and a plate (not shown) on displaceable element 11. A restoring force is applied to the displaceable element by a current flow through coils 17, 18. The generation of restoring current will be described below. Further details of such an accelerometer may be found in Jacobs U.S. patent 3,702,073.

A detector circuit 20 connected with capacitor plates 15, 16 has an analog output signal with a polarity which indicates the direction of displacement of element 11 and an amplitude which represents the magnitude of the displacement or other sensed stimulus. The detector output signal is connected with the input of an up-down accumulator 21 which increments for one polarity of detector output signal and decrements for the other polarity of detector output signal. An amplifier 22 may be connected between detector 20 and accumulator 21 to scale the analog signal, provide isolation between the detector and the accumulator and to provide frequency compensation should that be desirable.

Up-down accumulator 21 as shown in the drawing has a 16 bit output which provides a binary digital output representing the stimulus acting on the displaceable element 11. The accumulator output is nominally one-half full count for a null condition of the displaceable element 11, e.g., the absence of an acceleration. The binary digital output may be buffered to provide the appropriate signal amplitude and isolation. The buffer output is typically connected with a computer or other digital signal processing equipment.

The output of up-down accumulator 21 is also connected with the input of a bipolar digital-to-analog converter 25 which has a zero output for a half count of the 16 input bits. The analog output of digital-to-analog converter 25 is connected with forcer coils 17, 18 to return displaceable element to a null position.

Appropriate clock inputs are provided to the accumulator 21 and digital-to-analog converter 25. Amplifier 26 may be connected between the output of digital-to-analog converter 25 and forcer coils 17, 18 to scale the current to the coils and provide frequency compensation.

When accelerometer 10 senses acceleration, the analog output of detector 20 causes accumulator 21 to count up or down. The digital-to-analog converter 25 develops an analog rebalance current which returns the displaceable element 11 to its null position.

Accumulator 21 has a low noise output which is directly compatible with a digital computer. Null or zero input bias errors can be compensated in the buffer circuit by incorporating an add or subtract count circuit. As the instrument is designed to interface with a digital computer, this bias correction can also be provided by adding or subtracting counts in subsequent processing.

During temperature and acceleration modeling, errors of the detector, accumulator and converter can be modeled along with temperature and acceleration errors of the accelerometer 10. A composite correction is programmed for the computer with which the accelerometer is used.

The rebalance current typically required will be between counts of the accumulator and steps of the digital-to-analog converter 25. The 16 bit accumulator shown in the drawing provides a 16 bit output resolution which is approximately 1/4 mG in a 20G full range accelerometer. The two least significant bits of the binary digital output may be suppressed to avoid instability in the digital output, or the readings may be sampled and averaged to increase resolution beyond the nominal 16 bits. Since the servo loop forces the detector output to average zero over time, the LSB will be duty cycled to average proportionately between steps. As an additional advantage, the accumulator and digital-to-analog converter outputs will rattle or switch back and

forth the least significant bits. This does not affect the binary digital output. It has a beneficial effect with an instrument having a pivot and jewel mount rather than hinge shown in the drawing, in causing the displaceable element to dither about the null position. This reduces hysteresis and nonrepeatability errors.

Aliasing is an error which occurs when an instrument is read by a computer. Output changes are apparent to the computer only at transitions of the computer's clock. Normally the output of the instrument will change at some time other than the computer clock transition. If the time to a negative going output change of the instrument is 10.5 computer clock cycles, the time will appear to the computer as 10 clock cycles. If the time to the next positive going change is also 10.5 clock cycles it will appear to the computer as 11 clock cycles. If changes continue at this rate (some fraction of the computer clock rate) this gives an error in the apparent average output the computer sees.

This instrument may be syncronized with a system clock so that output transitions can occur only after an integer number of computer clock cycles. This eliminates aliasing and does not increase the average error, since if one transition is delayed, the error is stored as failure to totally rebalance the pendulum and some subsequent transition of this same polarity will occur sooner.

CLAIMS

1. A servoed instrument with a digital output, comprising:

an element displaceable in either of two opposite directions from a null position in response to a sensed stimulus;

means for applying a force to said element to return the element to said null position;

a detector responsive to displacement of said element from said null postition, having an analog output signal with a polarity which indicates the direction of displacement of said element from said null position and an amplitude which represents the magnitude of the sensed stimulus;

an analog-to-digital converter responsive to the detector output signal, having a digital output representing the sensed stimulus to which said element responds; and

a digital-to-analog converter having an input connected with the output of said analog-to-digital converter and an analog output connected with the means for applying a force to said element.

2. The instrument of claim 1 in which said analog-to-digital converter is an accumulator responsive to the detector output signal, having a binary digital output representing the sensed stimulus to which said element responds.

3. The instrument of claim 2 in which said accumulator is a counter which counts up for one polarity of detector output signal and counts down for the opposite polarity of detector output signal.

4. The instrument of claim 3 in which the output of said accumulator is one-half full count for a null condition in the absence of a stimulus acting on said displaceable element.

5. The instrument of claim 1 including an amplifier connected between said detector and said analog-to-digital converter.

6. The instrument of claim 5 in which said amplifier provides frequency compensation for the analog output signal from the detector.

7. The instrument of claim 1 in which said analog-to-digital converter has an n-bit output with the m most significant bits providing a digital measure of the sensed stimulus and the (n-m) least significant bits effecting dithering of the displaceable element.

8. The instrument of claim 1 including a buffer circuit connected with the output of the analog-to-digital converter for deriving a binary digital representation of the sensed stimulus therefrom.

9. The instrument of claim 8 in which said buffer circuit compensates the digital output signal for bias in the output of the instrument with a null condition of the sensed stimulus.

10. The instrument of claim 1 in which said digital-to-analog converter has a bipolar analog output.

11. The instrument of claim 10 in which said digital-to-analog converter has a zero analog output for one-half full scale digital input.

12. The instrument of claim 1 including an amplifier connected between the digital-to-analog converter and the force applying means.

13. The instrument of claim 10 including an amplifier connected between the digital-to-analog converter and the force applying means.

14. The instrument of claim 12 in which said amplifier provides frequency compensation for the analog output signal from the digital-to-analog converter.

15. The instrument of claim 13 in which said amplifier provides frequency compensation for the analog output signal from the digital-to-analog converter.

16. A servoed instrument with a binary digital output, comprising:

means for applying a force to said element to return the element to said null position;

a detector responsive to displacement of said element from said null position, having an analog output signal with a polarity which indicates the direction of displacement of said element from said null position and an amplitude which represents the magnitude of the sensed stimulus;

an accumulator responsive to the detector output signal, having a binary digital output representing the sensed stimulus to which said element responds, said accumulator incrementing for one polarity of output signal and decrementing for the opposite polarity of output signal and the output of said accumulator being one-half full count in the absence of a stimulus acting on said displaceable element; and

a digital to analog converter having an input connected with the output of said analog-to-digital

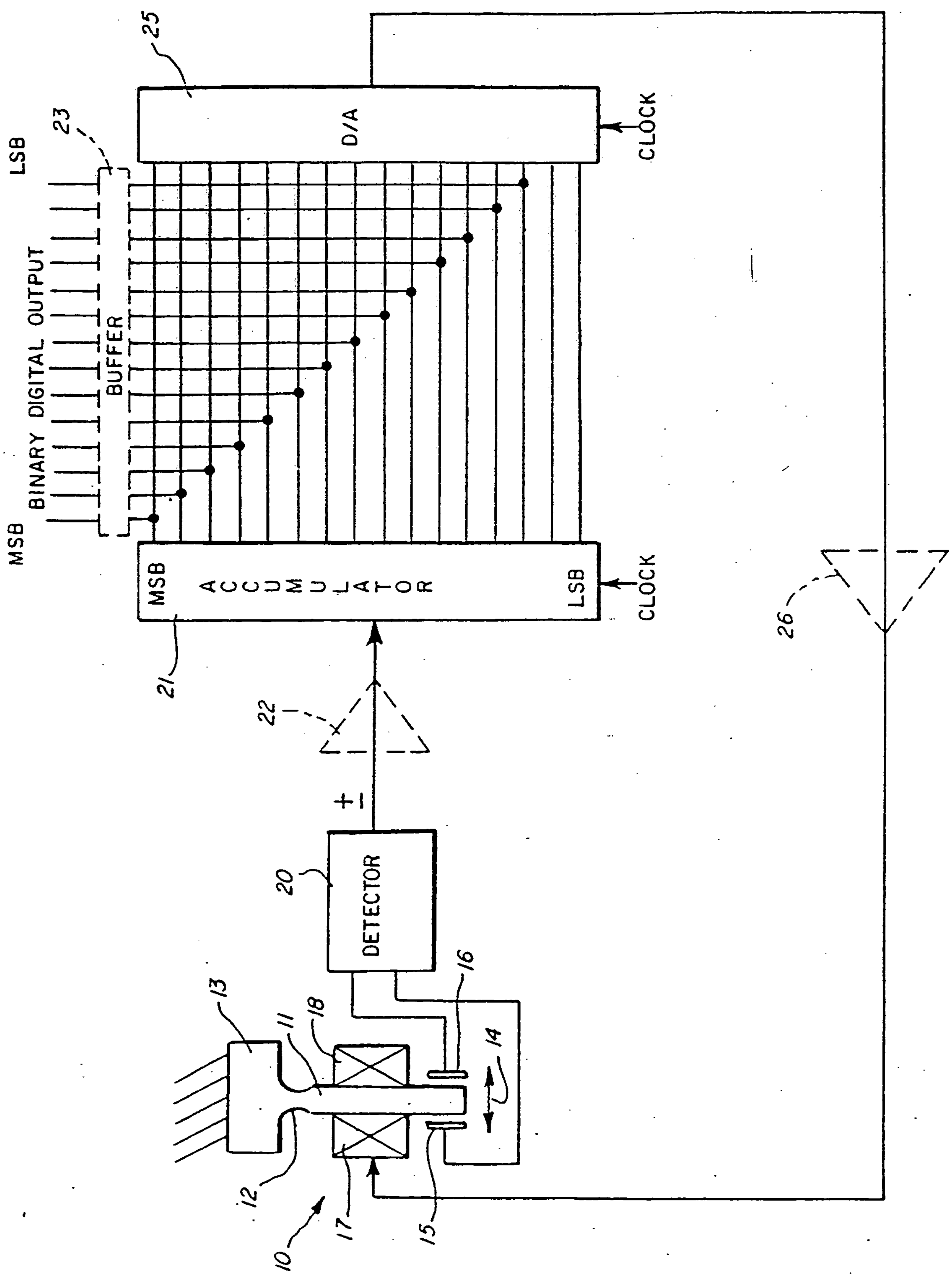
converter and a bipolar analog output connected with the means for applying a force to said element, one-half full scale digital input corresponding with a zero analog output from said digital-to-analog converter.

17. In a servoed accelerometer having a mass movable in opposite directions from a null position in response to accelerations and means for applying a rebalance force to the mass, a digital output circuit comprising:

a detector responsive to displacement of said mass from said null position having an analog output signal with a polarity which indicates the direction of the acceleration and an amplitude which represents the intensity thereof;

an analog-to-digital converter responsive to the analog detector output signal having a digital output representing the sensed acceleration; and

a digital-to-analog converter having an input connected with the output of said analog-to-digital converter and an analog output connected with the means for applying a restoring force to the mass.


25
D/A
CLOCK
23
LSB
BINARY DIGITAL OUTPUT
BUFFER
MSB
MSB
ACCUMULATOR
LSB
CLOCK
21
22
+
-
20
DETECTOR
26
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11
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16
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15

INTERNATIONAL SEARCH REPORT

International Application No PCT/US85/01143

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [3]

According to International Patent Classification (IPC) or to both National Classification and IPC

INT. CL.[3] G01P 15/13

U.S. CL. 73/ 517B; 318/648,651

II. FIELDS SEARCHED

Minimum Documentation Searched [4]

Classification System	Classification Symbols
U.S.	73/517B 318/601, 648,651

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [5]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [14]

Category *	Citation of Document, [16] with indication, where appropriate, of the relevant passages [17]	Relevant to Claim No. [18]
X,Y	US,A, 3,081,637, 19 March 1963, Gevas.	1-17
X,Y	US,A, 3,192,371, 29 June 1965, See Figure 4, Brahm.	1-17
X,Y	US,A, 4,282,470, 04 August 1981, Reynolds.	1-17
Y	US,A, 3,618,401, 09 November 1971, Lacey.	5,12-13
Y	US,A, 3,508,254, 21 April 1970, Ross et al.	7
Y	US,A, 4,315,434, 16 February 1982, Eastman.	7
Y	US,A, 3,545,284, 08 December 1970, Clement et al.	4,11 and 16

* Special categories of cited documents: [15]

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IV. CERTIFICATION

Date of the Actual Completion of the International Search [2]	Date of Mailing of this International Search Report [2]
15 July 1985	23 JUL 1985
International Searching Authority [1]	Signature of Authorized Officer [20]
ISA/US	John E. Chapman, Jr.

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